PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/720,123
Filing Date:	November 25, 2003
Applicant:	Hoi-Jin Lee
Group Art Unit:	2138
Examiner:	John P. Trimmings
Title:	SEMICONDUCTOR DEVICE WITH SPEED BINNING TEST CIRCUIT AND TEST METHOD THEREOF
Attorney Docket:	2557-000191/US

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Mail Stop RCE

February 28, 2007

AMENDMENT UNDER 37 C.F.R. §1.114

Sir:

In response to the Final Office Action mailed July 28, 2006, and with the concurrently filed RCE, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

Amendments to the Claims begin on page 2 of this Amendment.

Remarks begin on page 8 of this Amendment.

	Claims remaining after Amendment		**Highest number previously paid for**		**Present extra**
Total	21	-	25	=	0
Independent	3	-	3	=	0